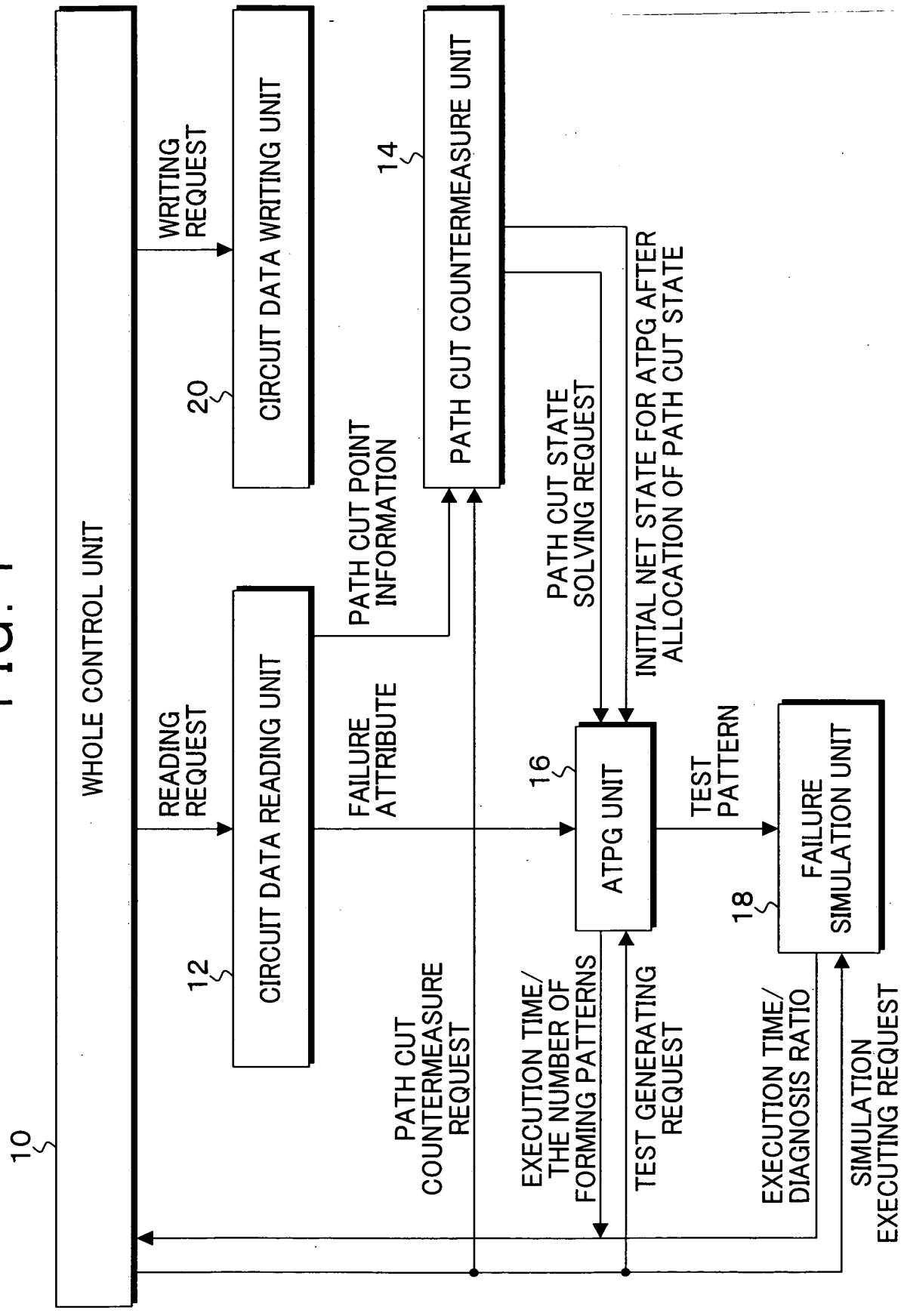
Title: INTEGRATED CIRCUIT TESTING METHOD, PROGRAM, STORING MEDIUM, AND APPARATUS
Inventor: Daisuke MARUYAMA
Appln. No.: Unknown
Docket No.: 108131-00004

FIG. 1



Title: INTEGRATED CIRCUIT TESTING METHOD, PROGRAM, STORING MEDIUM, AND APPARATUS
Inventor: Daisuke MARUYAMA
Appln. No.: Unknown
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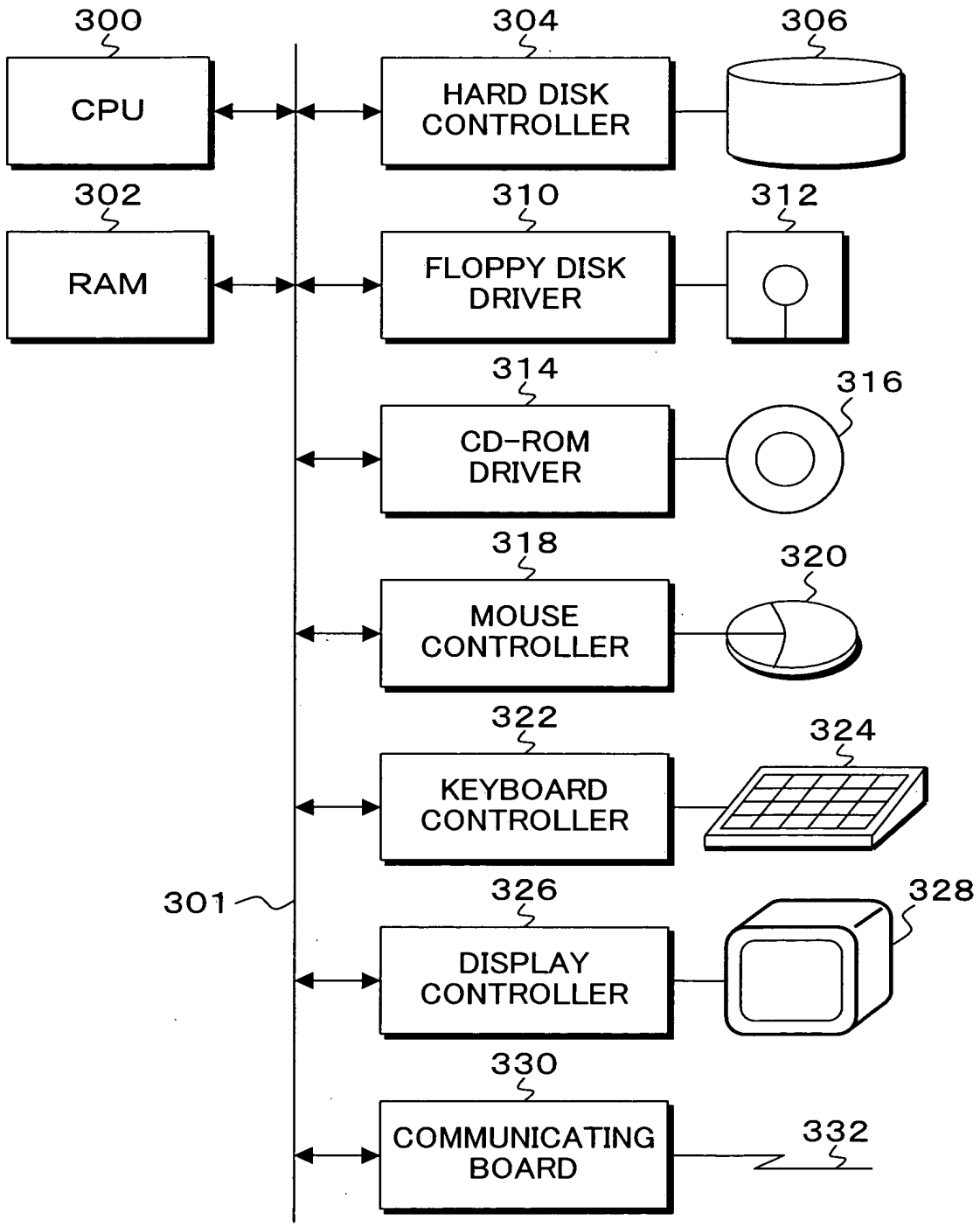
FIG. 2



Title: INTEGRATED CIRCUIT TESTING METHOD, PROGRAM, STORING MEDIUM, AND APPARATUS
Inventor: Daisuke MARUYAMA
Appln. No.: Unknown
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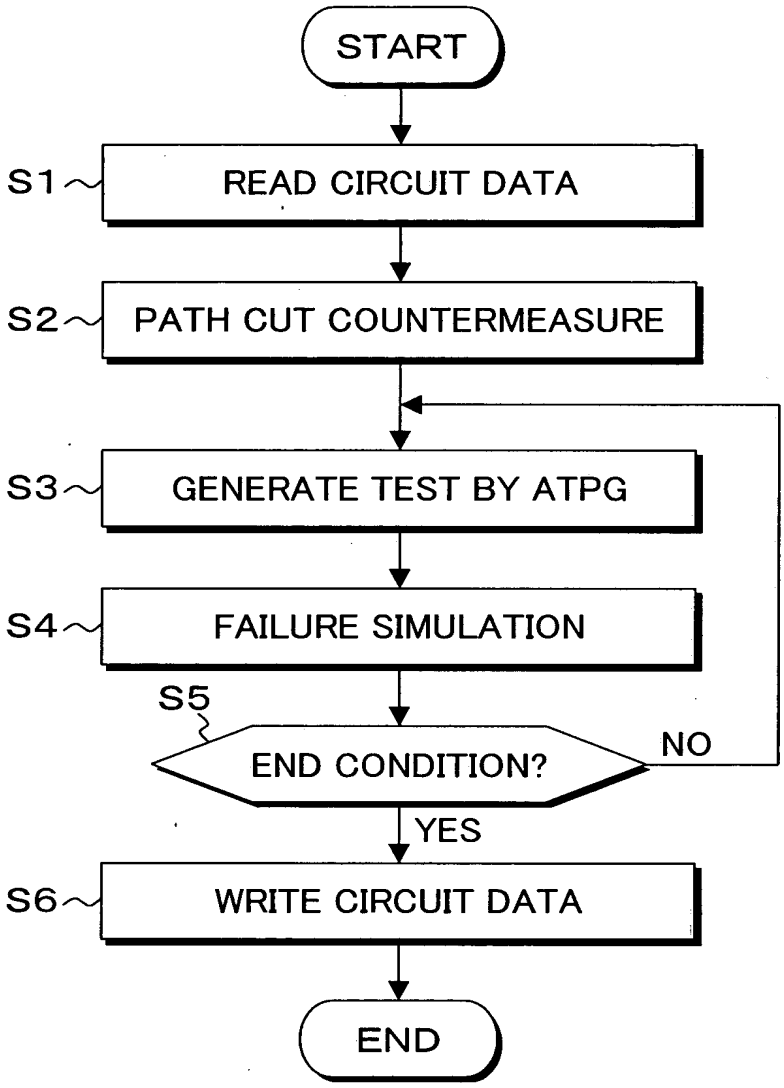
FIG. 3



Title: INTEGRATED CIRCUIT TESTING METHOD, PROGRAM, STORING MEDIUM, AND APPARATUS
Inventor: Daisuke MARUYAMA
Appln. No.: Unknown
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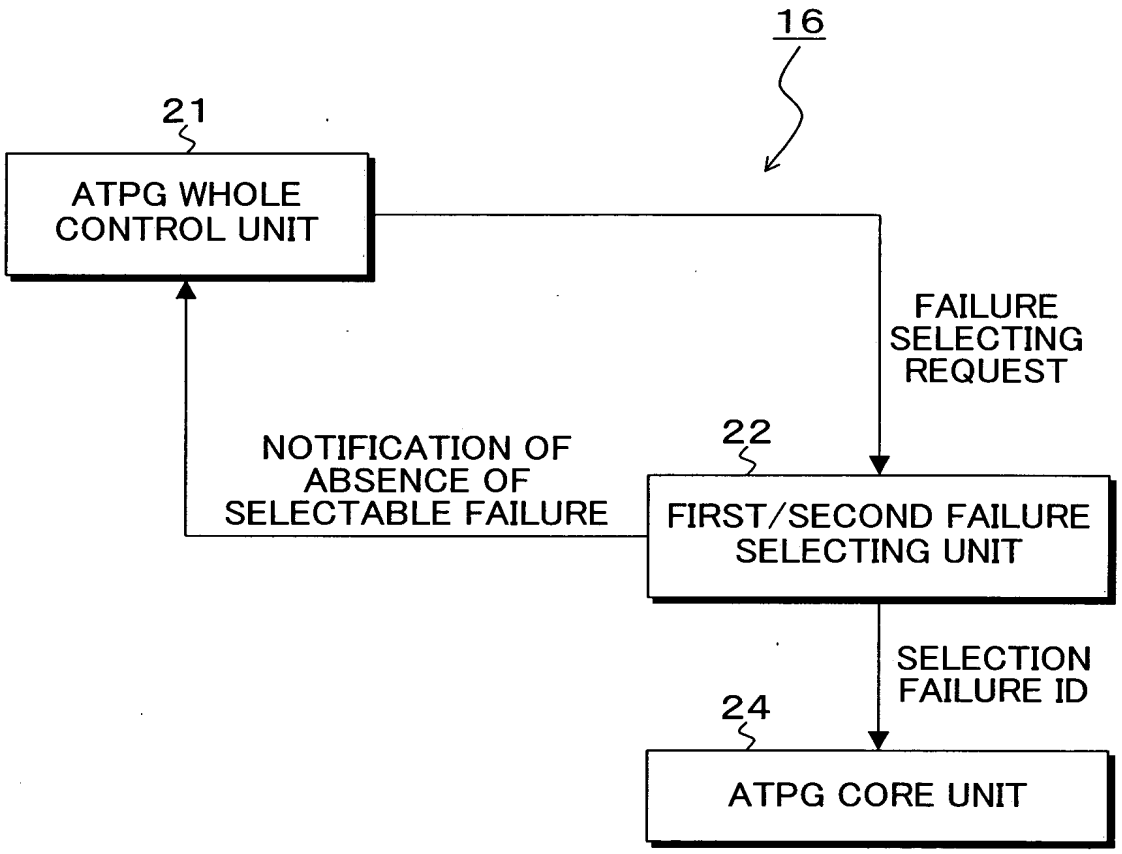
FIG. 4



Title: INTEGRATED CIRCUIT TESTING METHOD, PROGRAM, STORING MEDIUM, AND APPARATUS
Inventor: Daisuke MARUYAMA
Appln. No.: Unknown
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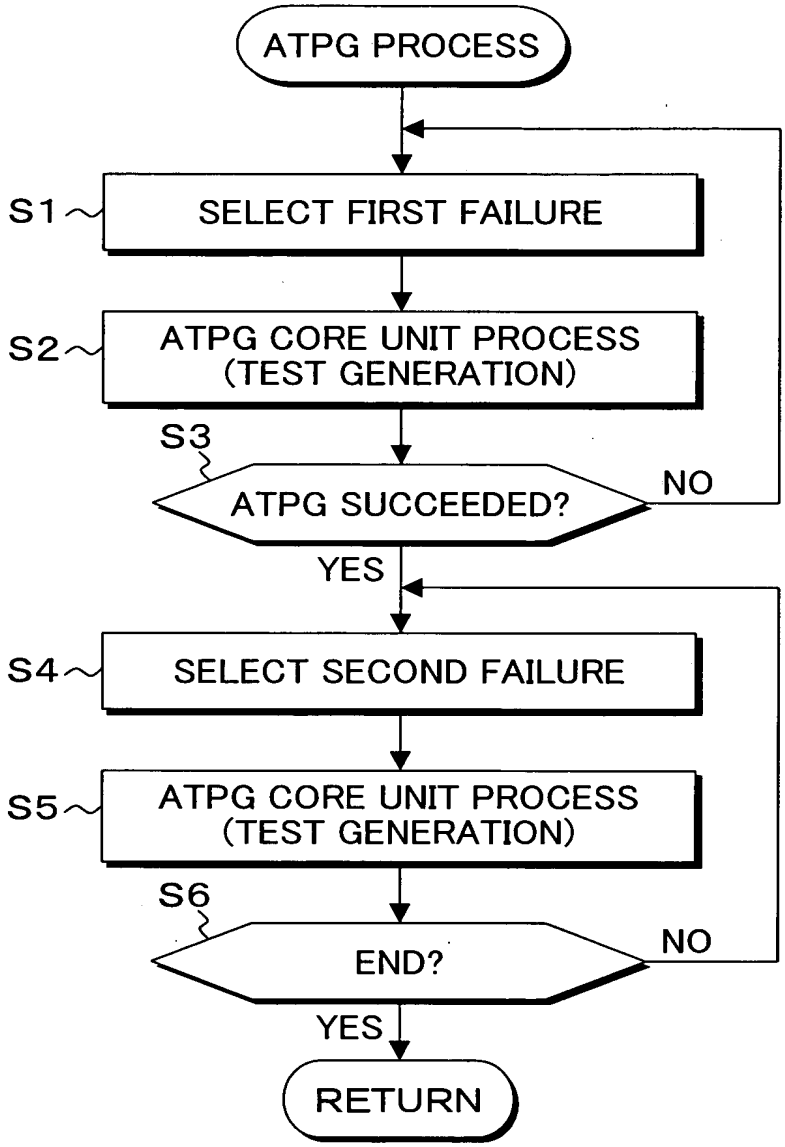
FIG. 5



Title: INTEGRATED CIRCUIT TESTING METHOD, PROGRAM, STORING MEDIUM, AND APPARATUS
Inventor: Daisuke MARUYAMA
Appln. No.: Unknown
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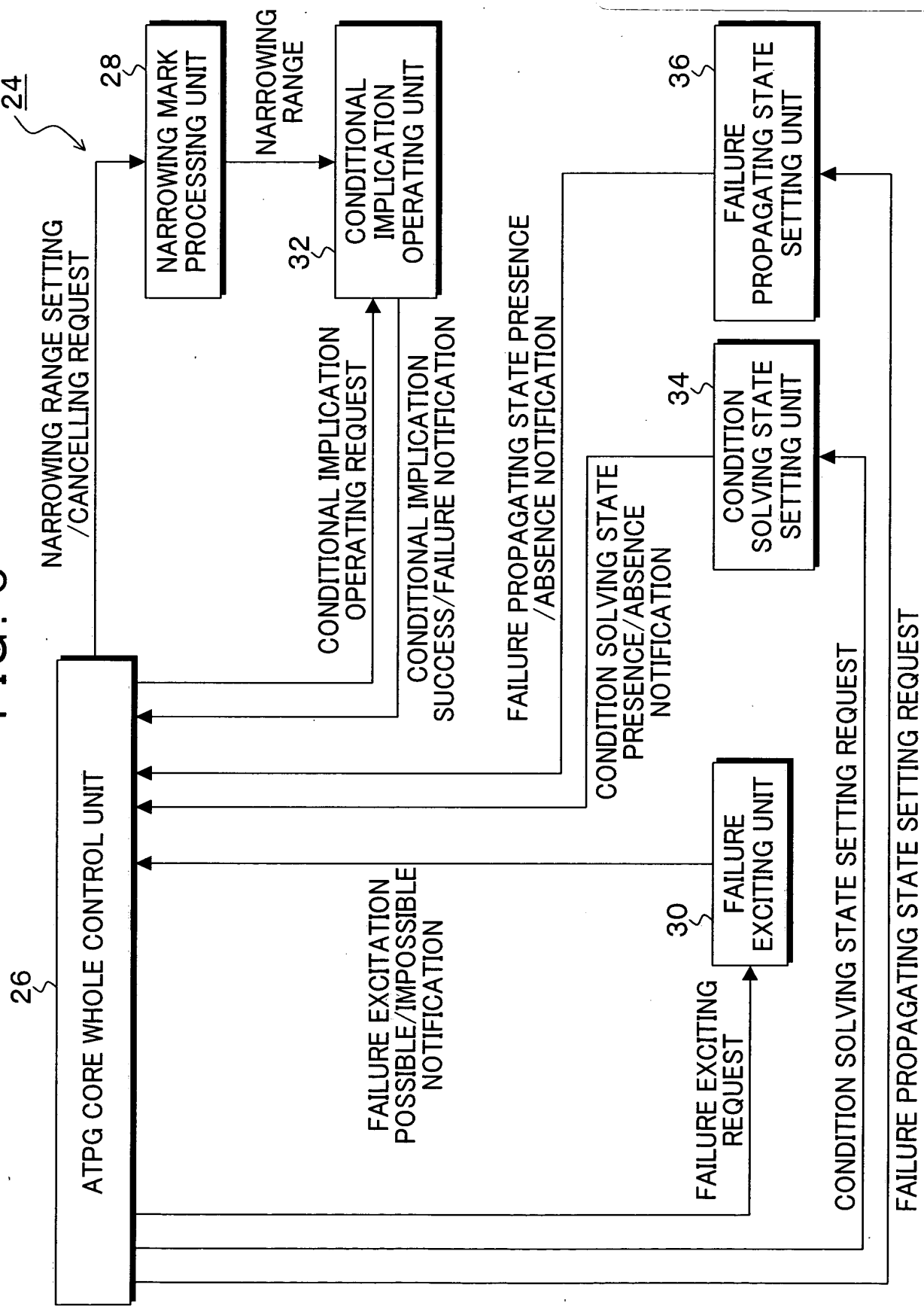
FIG. 6



Title: INTEGRATED CIRCUIT TESTING METHOD, PROGRAM, STORING MEDIUM, AND APPARATUS
Inventor: Daisuke MARUYAMA
Appln. No.: Unknown
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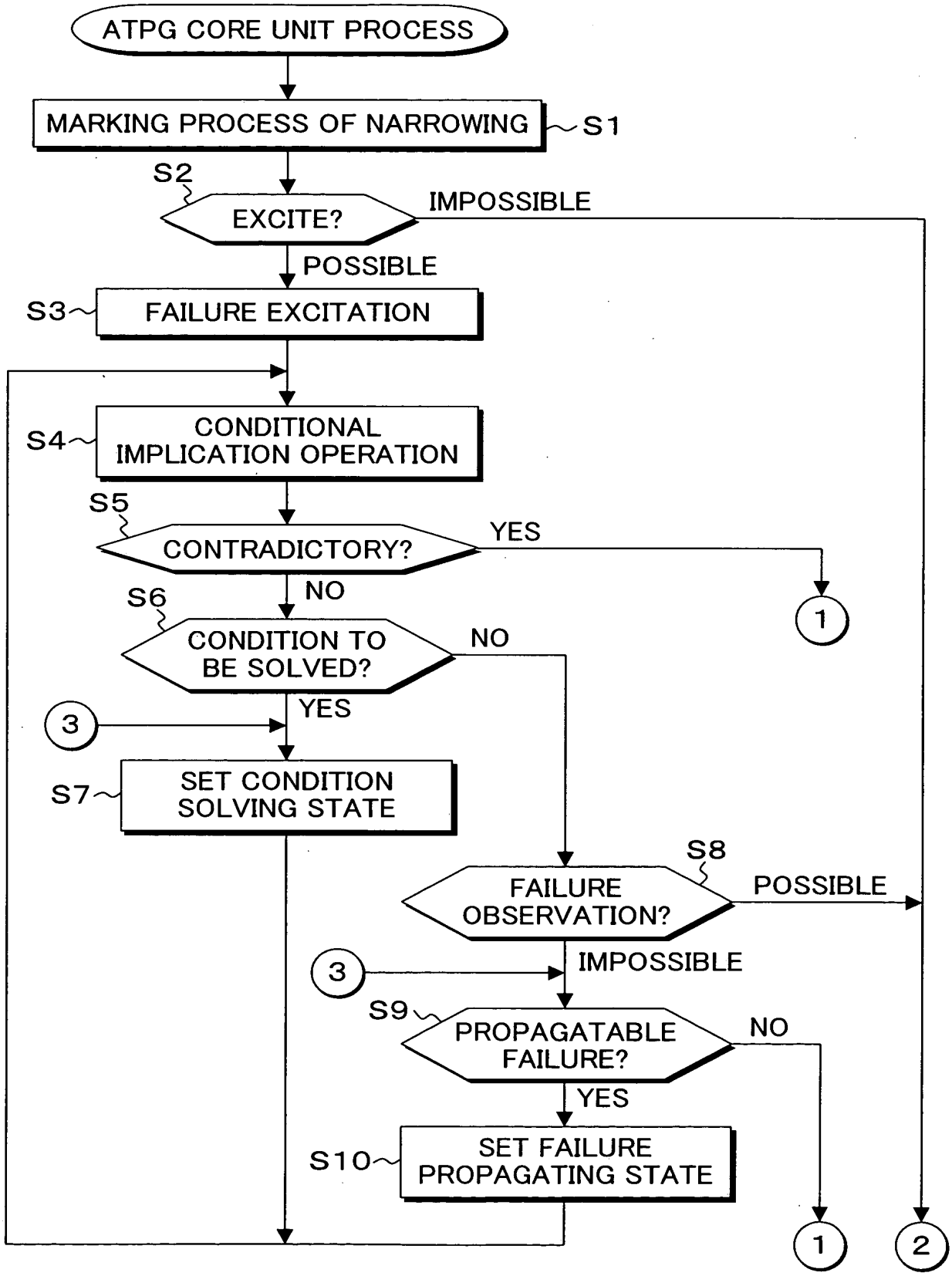
FIG. 7A



Title: INTEGRATED CIRCUIT TESTING METHOD, PROGRAM, STORING MEDIUM, AND APPARATUS
Inventor: Daisuke MARUYAMA
Appln. No.: Unknown
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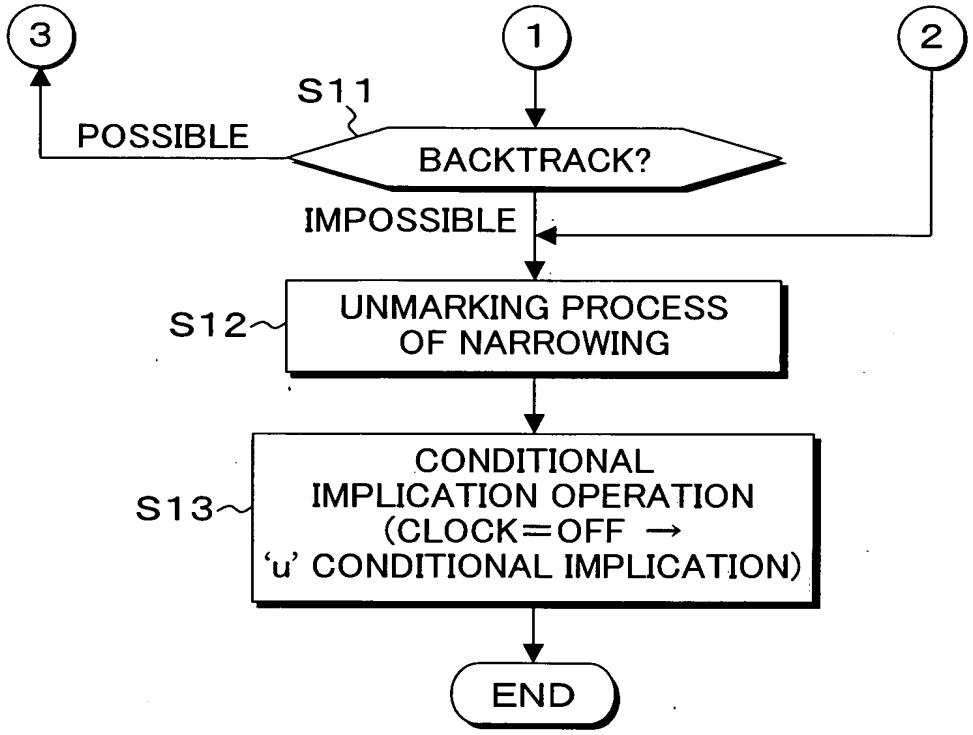
FIG. 7B



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Inventor: Daisuke MARUYAMA
Appln. No.: Unknown
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FIG. 8

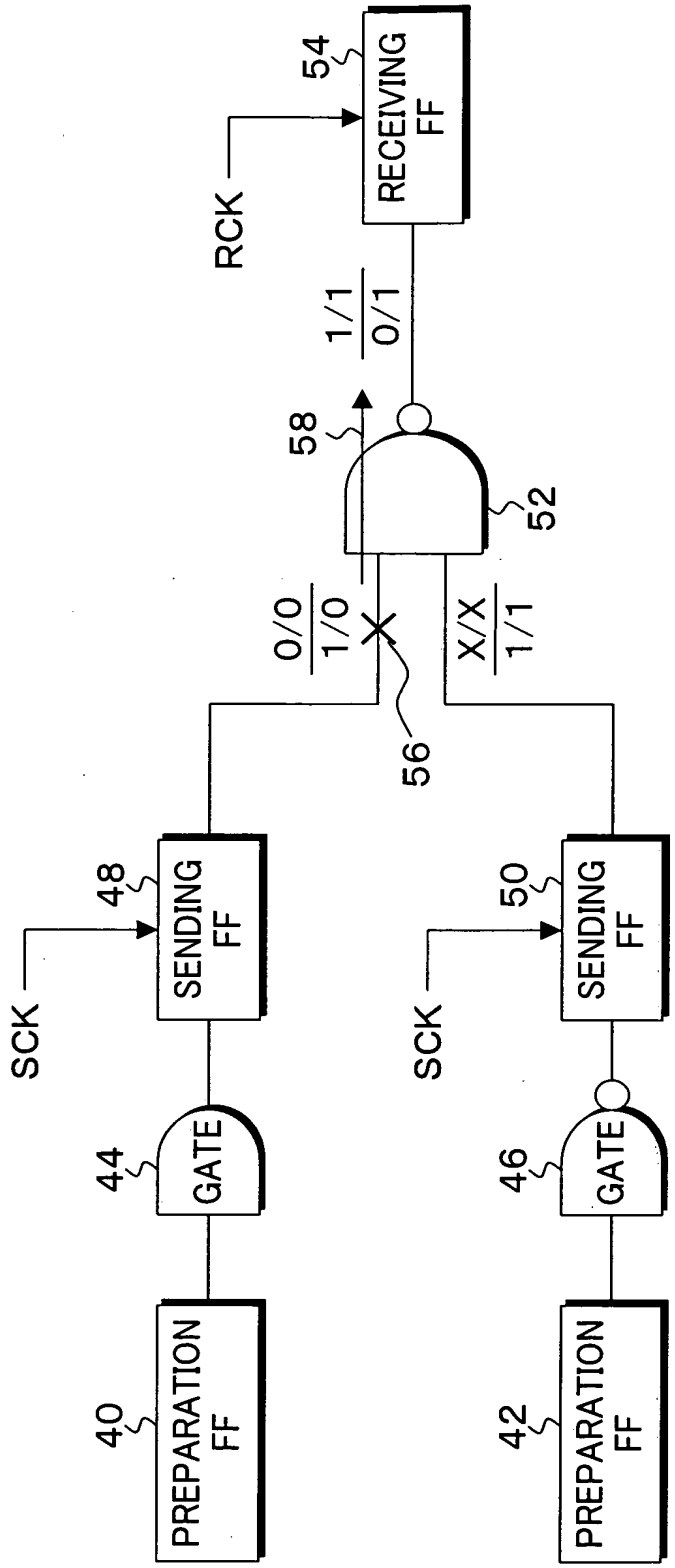

FIG. 9A

LEADING FAILURE EXCITATION

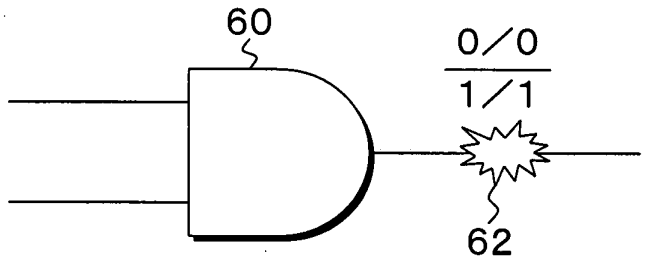

FIG. 9B

NORMAL

FIG. 9C

DELAY FAILURE

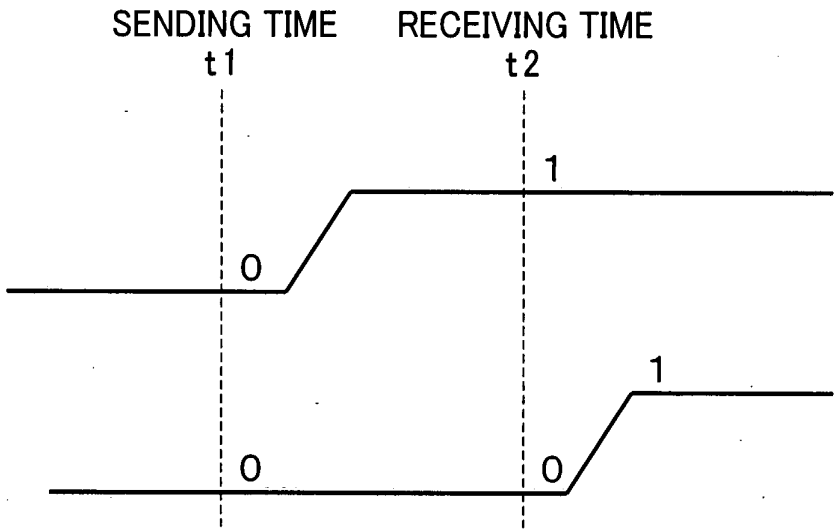

FIG. 9D

NOTATION

$$\frac{\text{SENDING TIME NORMAL VALUE/SENDING TIME FAILURE VALUE}}{\text{RECEIVING TIME NORMAL VALUE/RECEIVING TIME FAILURE VALUE}} = \frac{0/0}{1/0}$$

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Inventor: Daisuke MARUYAMA
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FIG. 10A

TRAILING FAILURE EXCITATION

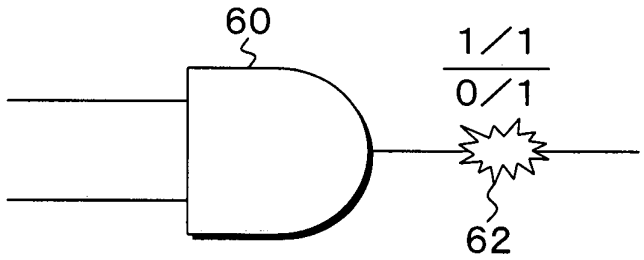

FIG. 10B

NORMAL

FIG. 10C

DELAY FAILURE

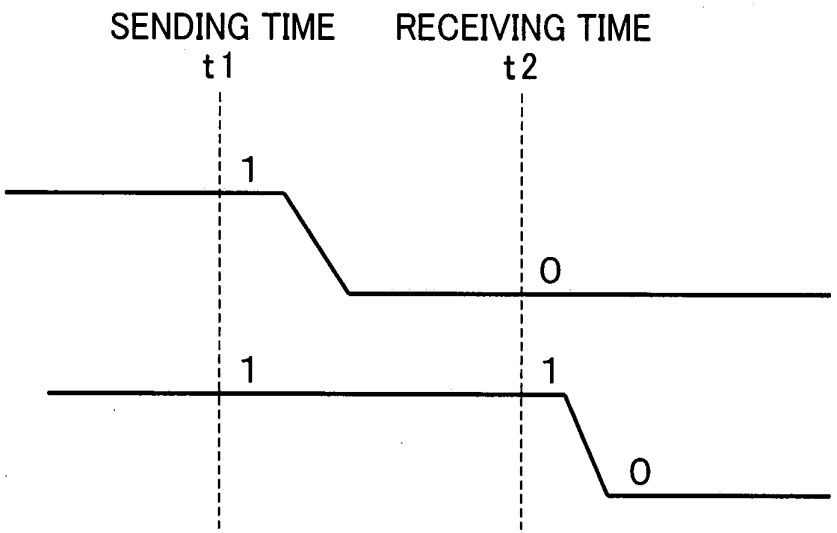

FIG. 10D

NOTATION

$$\frac{\text{SENDING TIME NORMAL VALUE/SENDING TIME FAILURE VALUE}}{\text{RECEIVING TIME NORMAL VALUE/RECEIVING TIME FAILURE VALUE}} = \frac{1/1}{0/1}$$

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Inventor: Daisuke MARUYAMA
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FIG. 11A

FIG. 11B

FIG. 11C

FIG. 11D

FIG. 11E

FIG. 11F

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Inventor: Daisuke MARUYAMA
Appln. No.: Unknown
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FIG. 12A

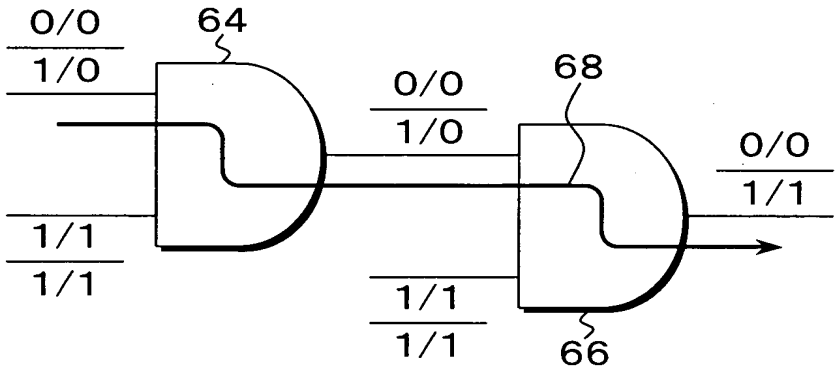
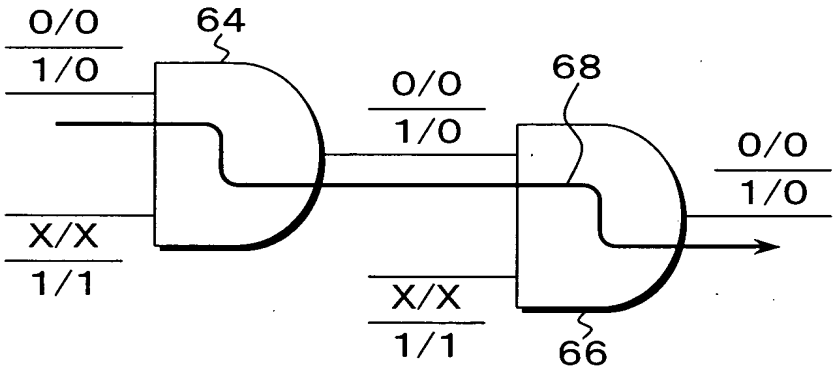


FIG. 12B



Title: INTEGRATED CIRCUIT TESTING METHOD, PROGRAM, STORING MEDIUM, AND APPARATUS
Inventor: Daisuke MARUYAMA
Appln. No.: Unknown
Docket No.: 108131-00004

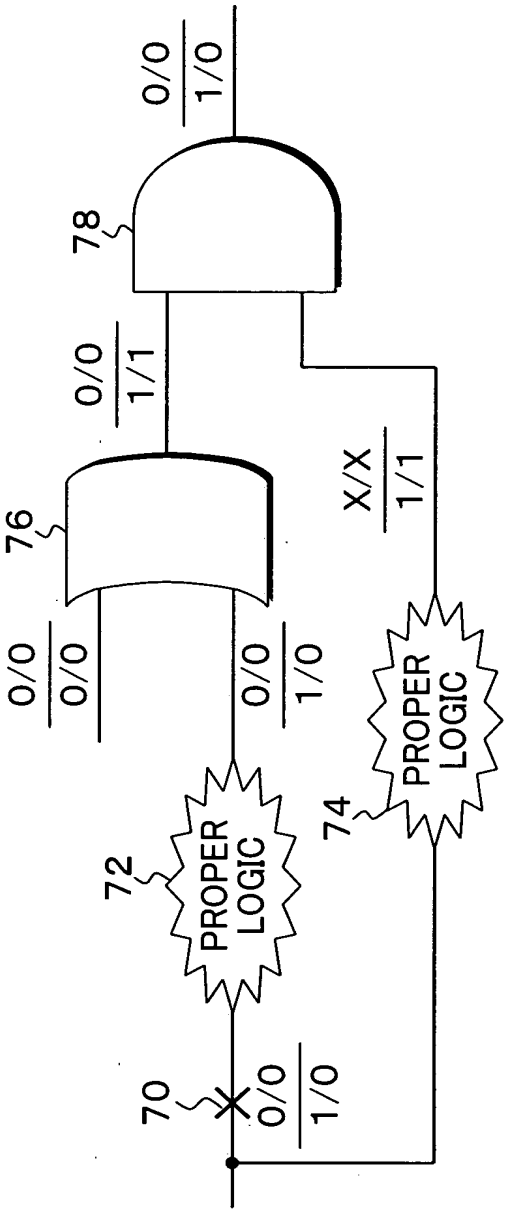


FIG. 13A

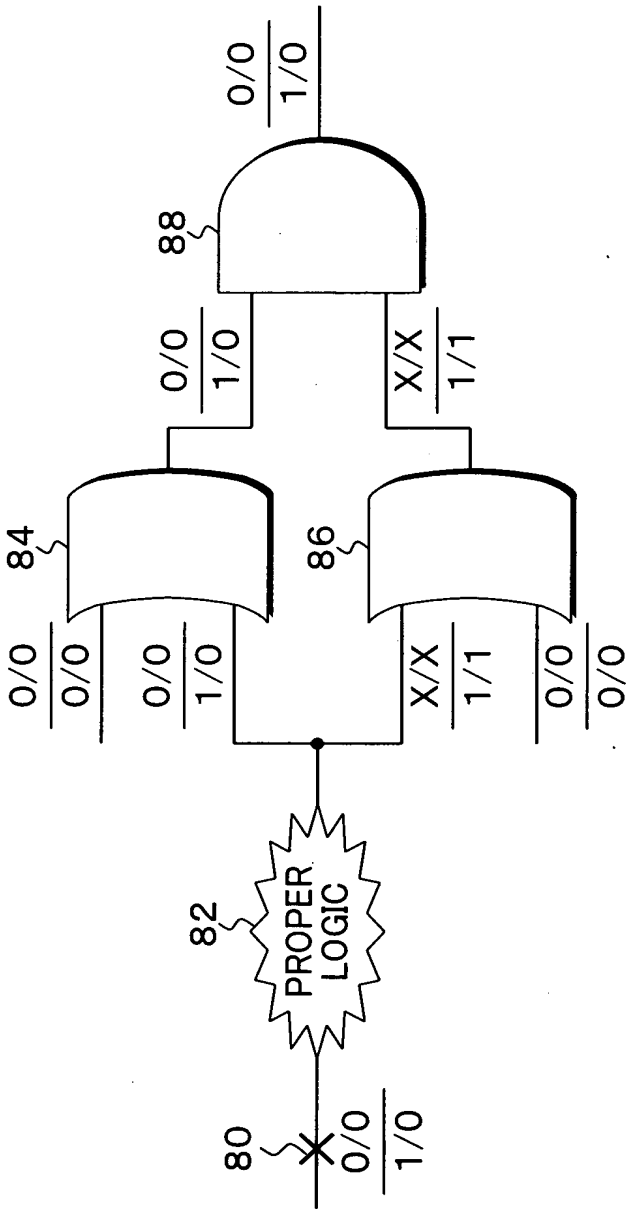


FIG. 13B

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Inventor: Daisuke MARUYAMA
Appln. No.: Unknown
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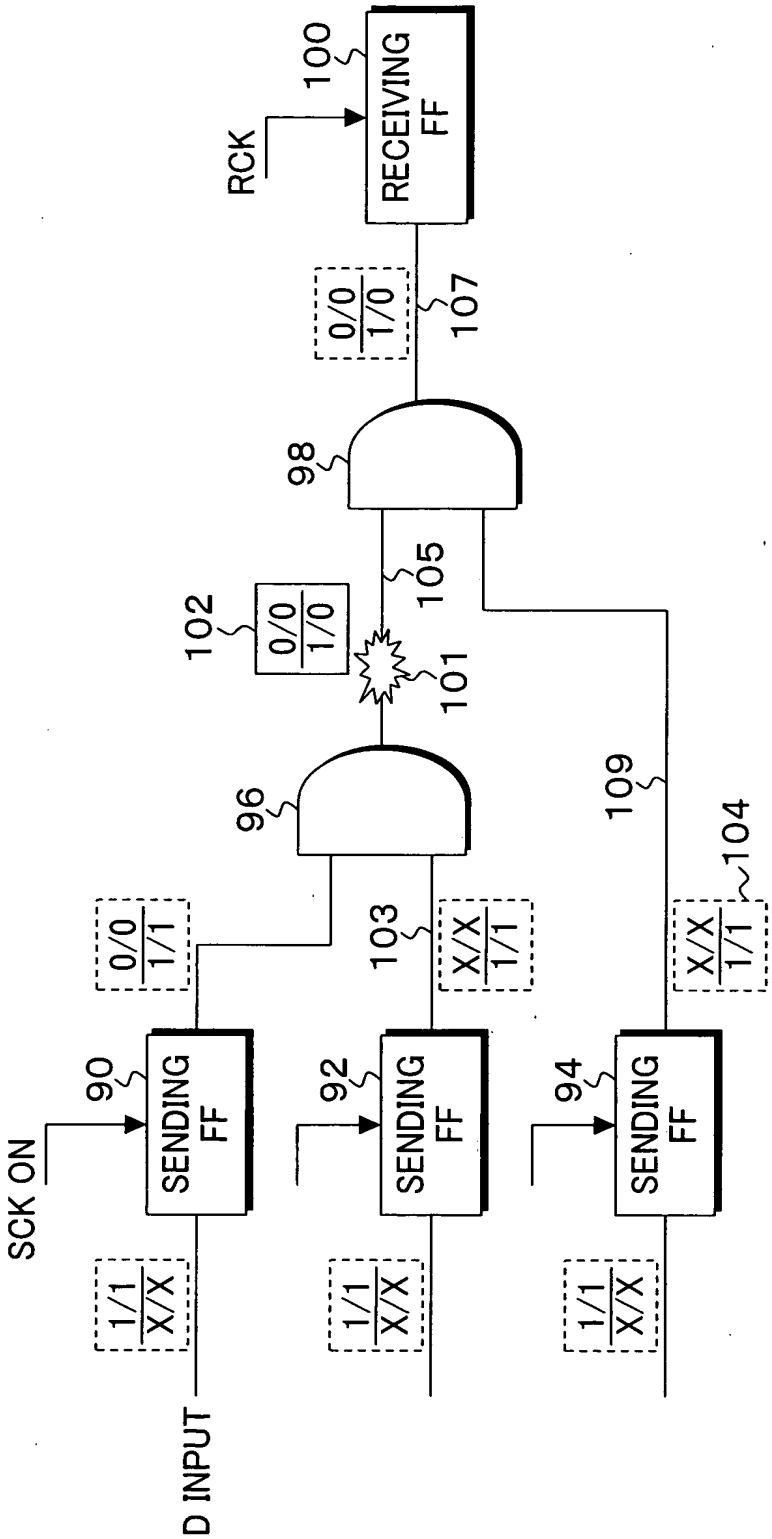
FIG. 14A



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Inventor: Daisuke MARUYAMA
Appln. No.: Unknown
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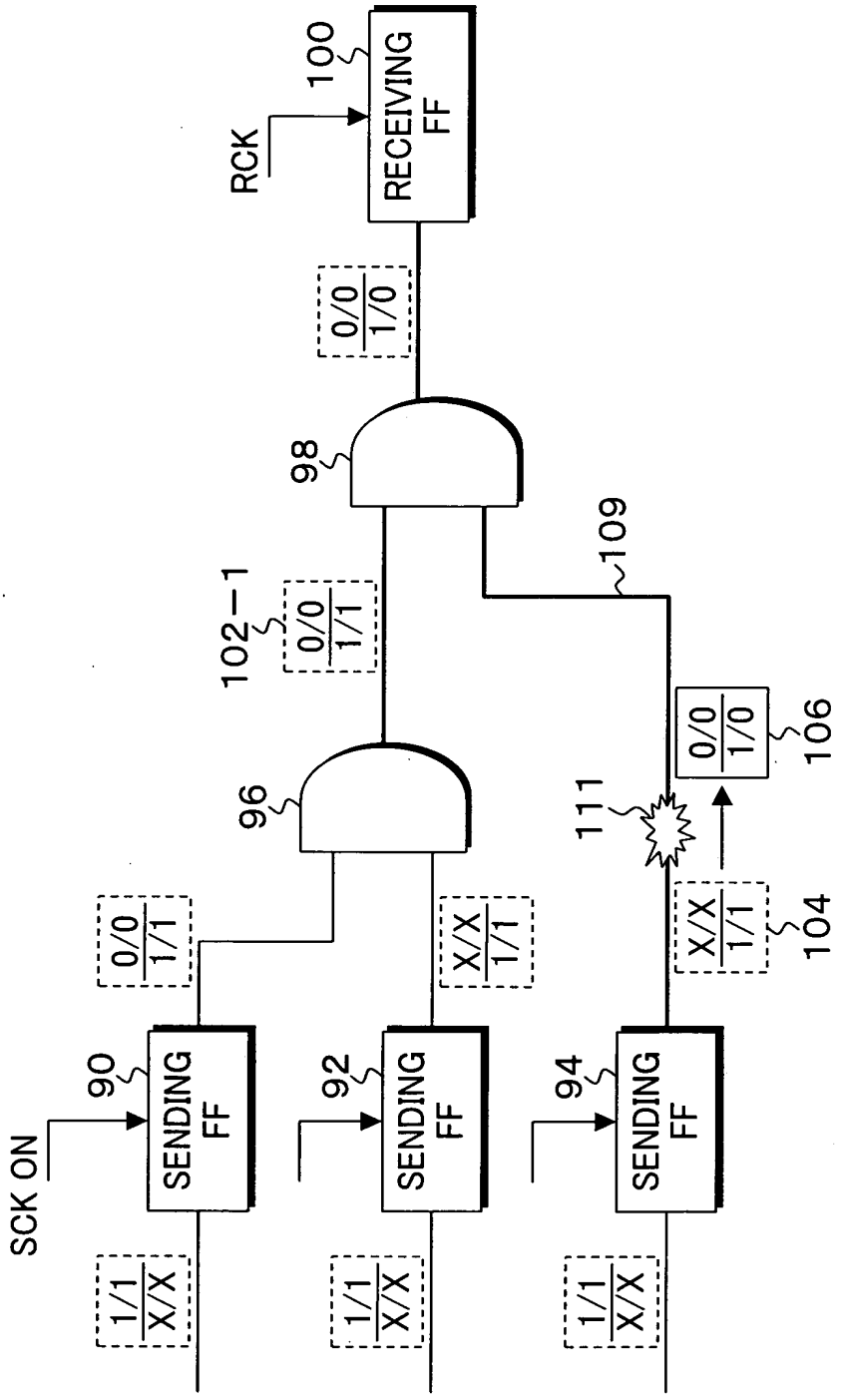
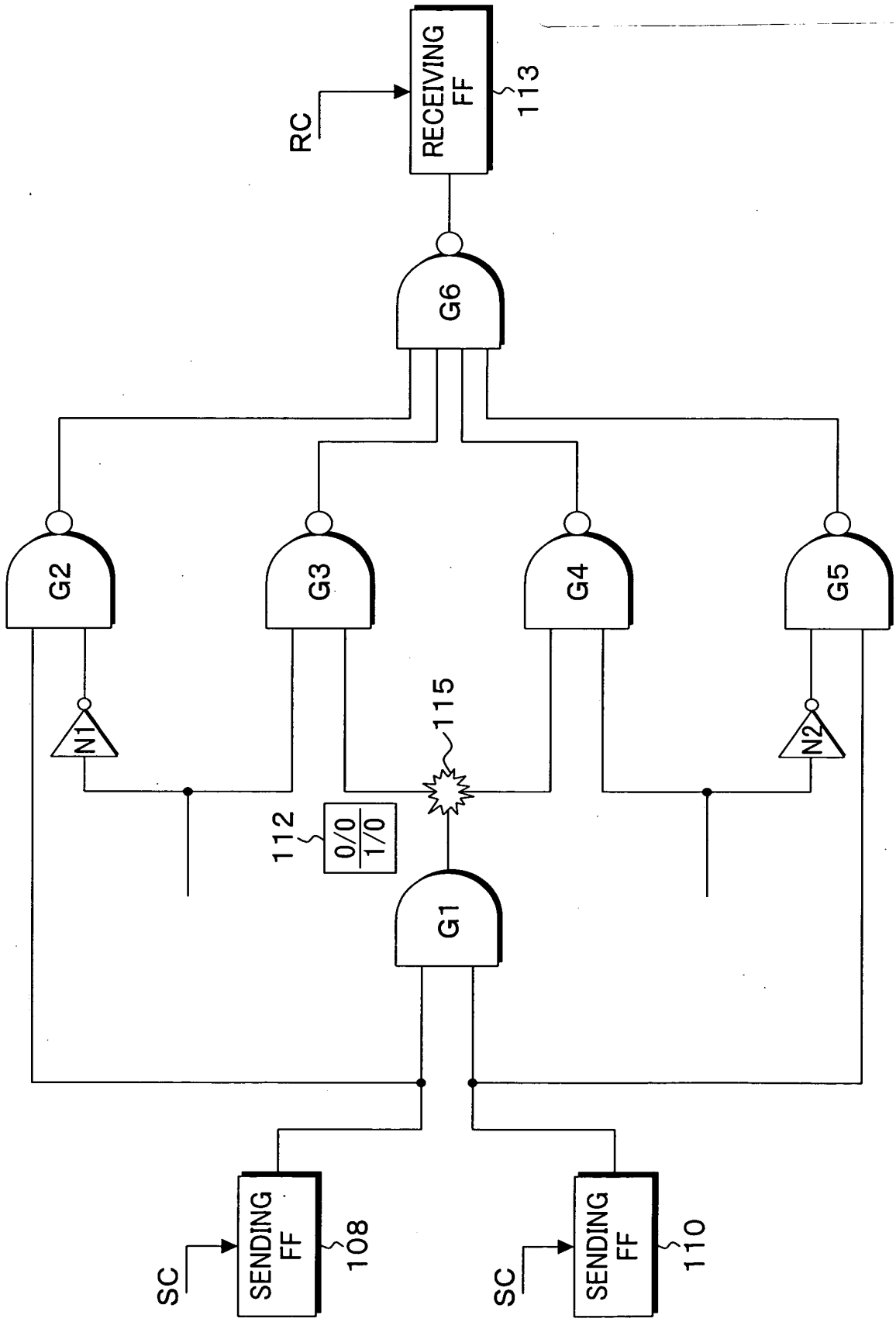
FIG. 14B



Title: INTEGRATED CIRCUIT TESTING METHOD, PROGRAM, STORING MEDIUM, AND APPARATUS
Inventor: Daisuke MARUYAMA
Appln. No.: Unknown
Docket No.: 108131-00004

FIG. 15



Title: INTEGRATED CIRCUIT TESTING METHOD, PROGRAM, STORING MEDIUM, AND APPARATUS
Inventor: Daisuke MARUYAMA
Appln. No.: Unknown
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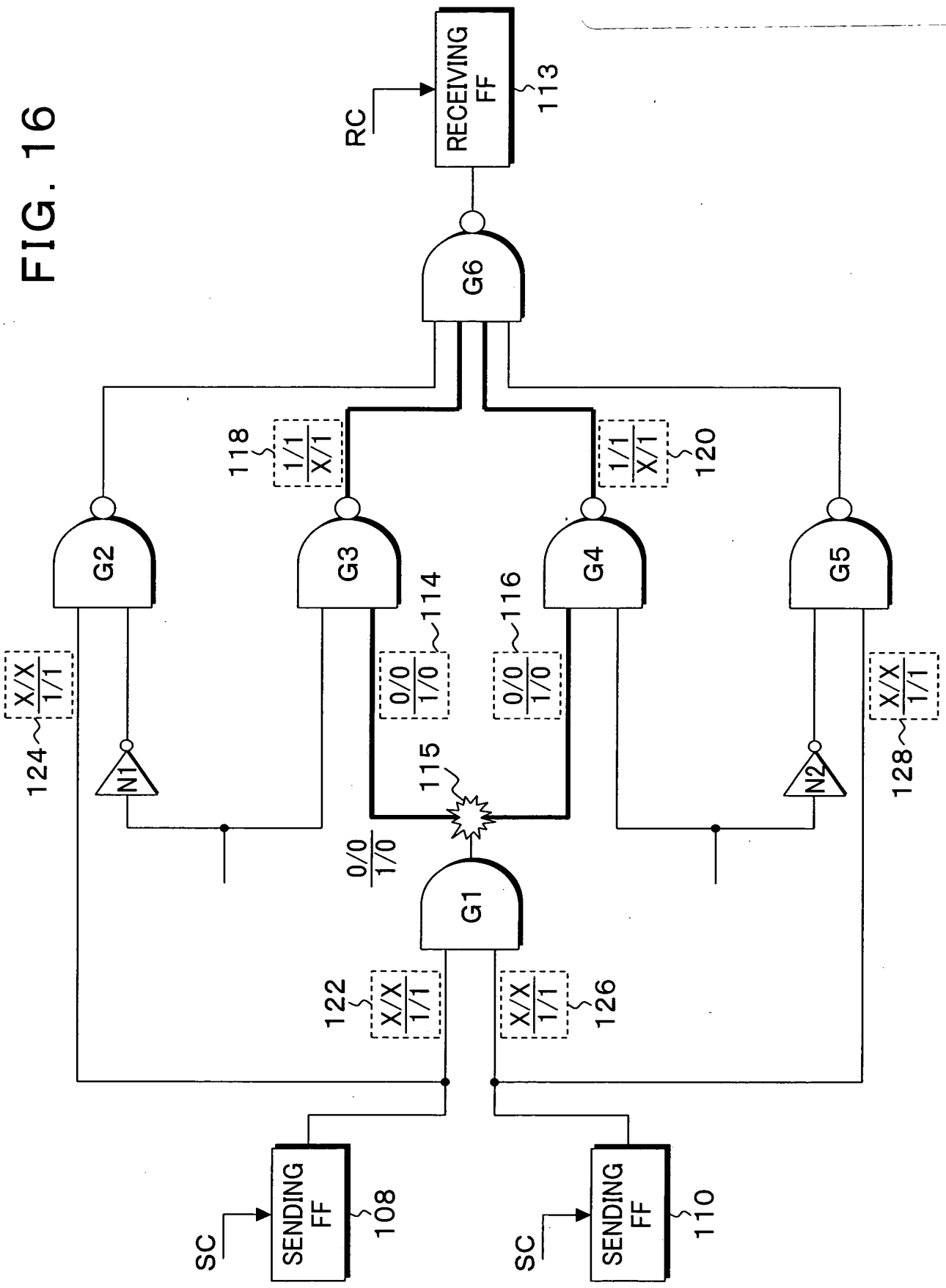
FIG. 16



Title: INTEGRATED CIRCUIT TESTING METHOD, PROGRAM, STORING MEDIUM, AND APPARATUS
Inventor: Daisuke MARUYAMA
Appln. No.: Unknown
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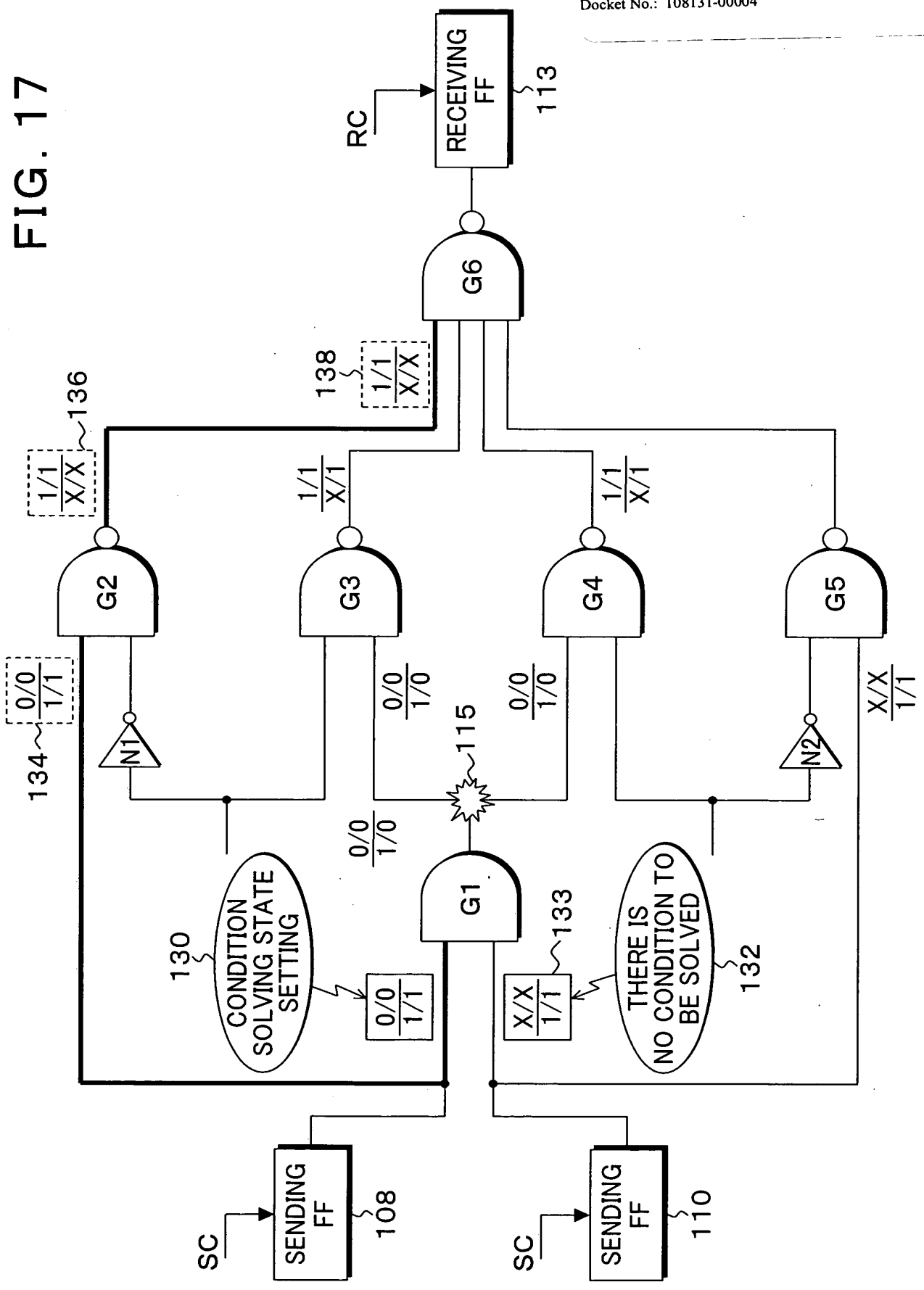
FIG. 17



Title: INTEGRATED CIRCUIT TESTING METHOD, PROGRAM, STORING MEDIUM, AND APPARATUS
Inventor: Daisuke MARUYAMA
Appln. No.: Unknown
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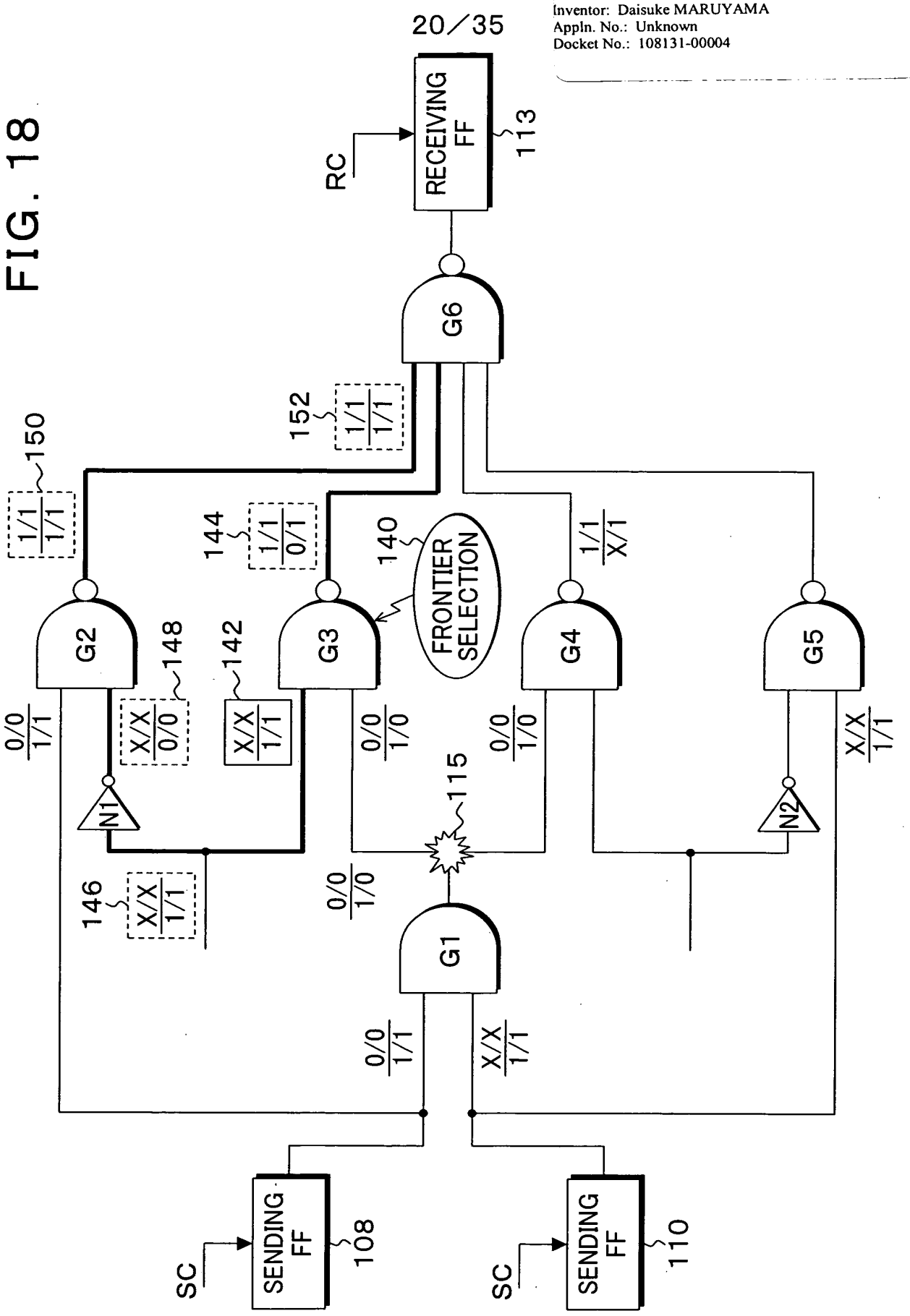
FIG. 18



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Inventor: Daisuke MARUYAMA
Appln. No.: Unknown
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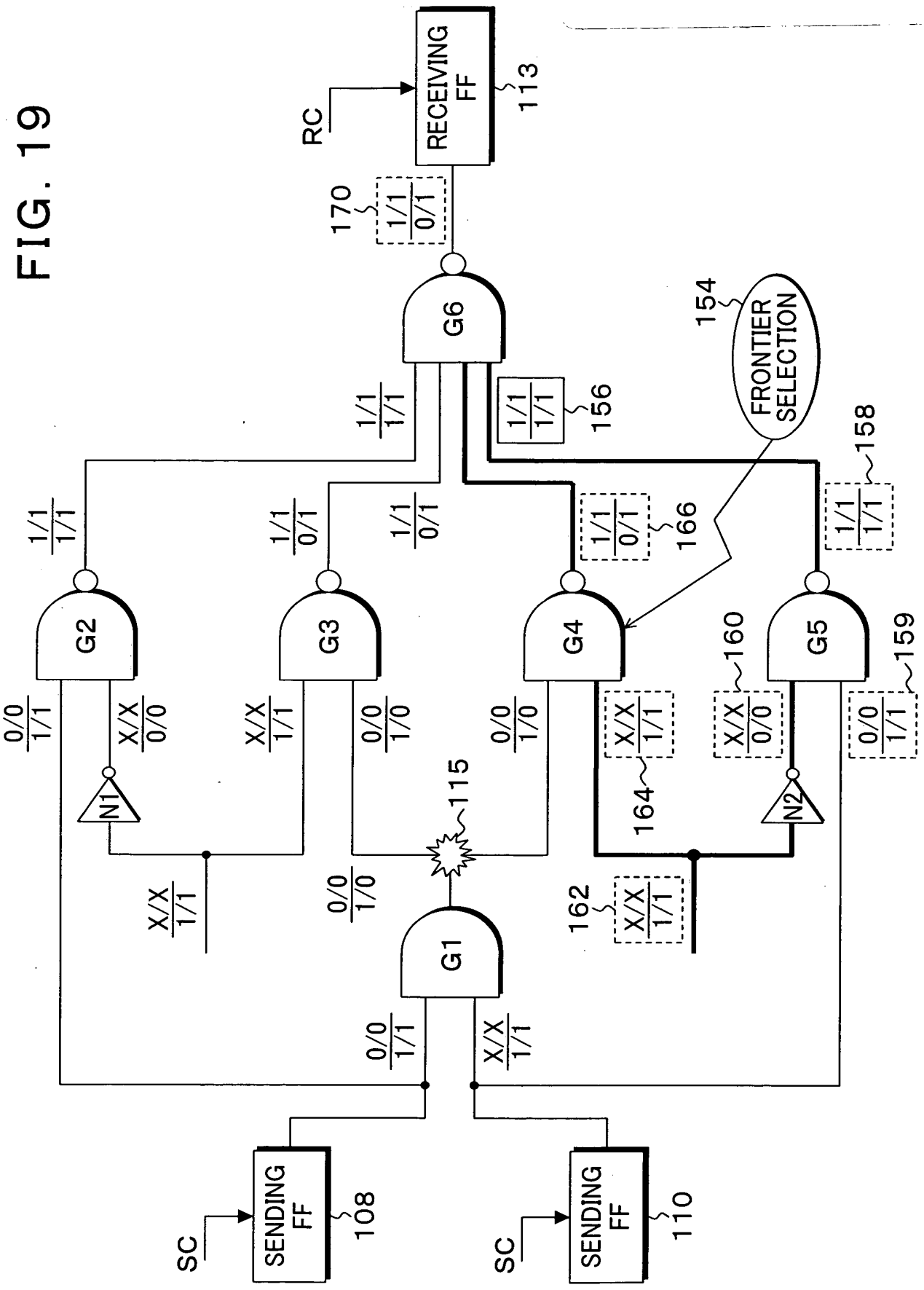
FIG. 19



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Inventor: Daisuke MARUYAMA
Appln. No.: Unknown
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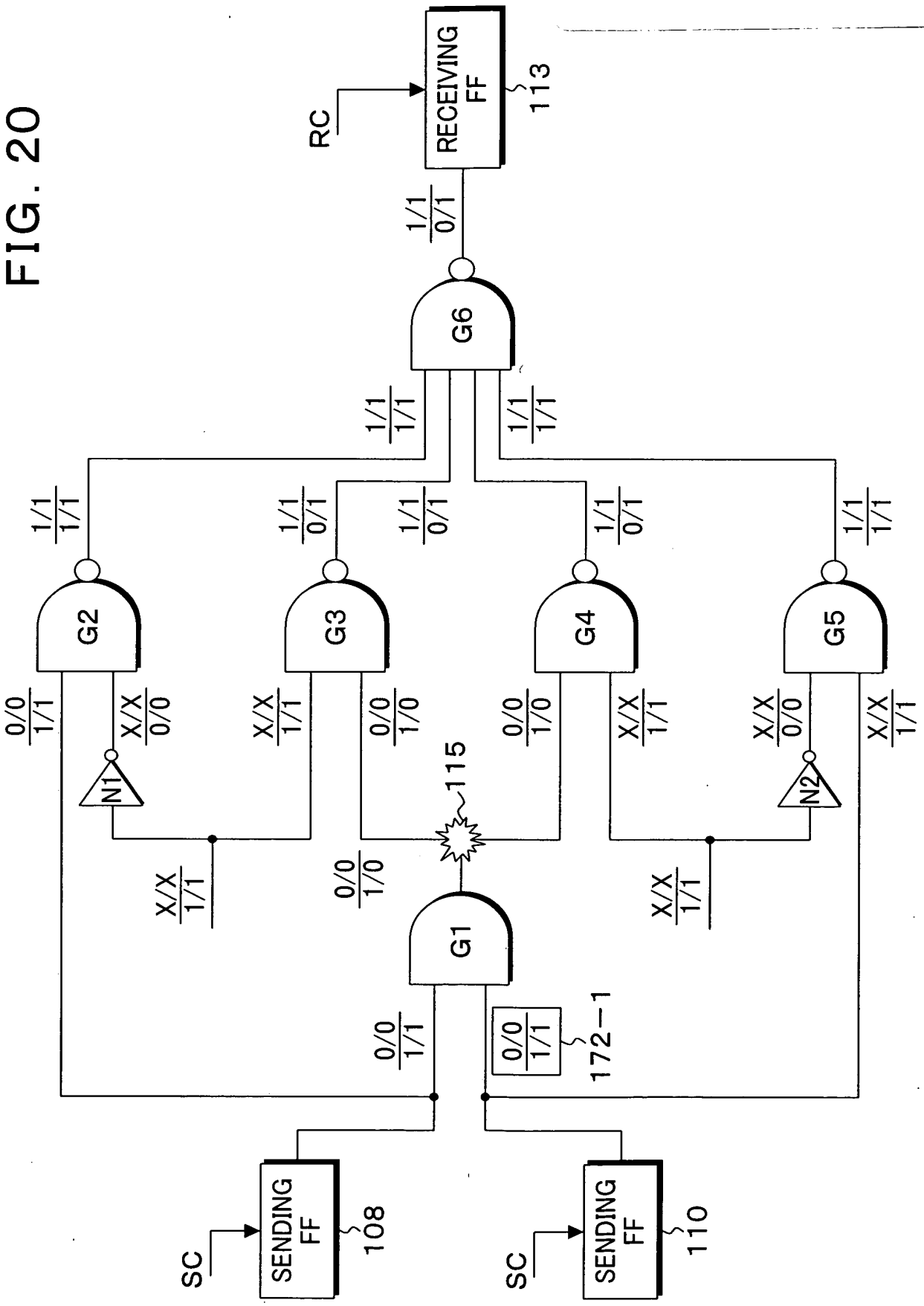
FIG. 20



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Inventor: Daisuke MARUYAMA
Appln. No.: Unknown
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FIG. 21A

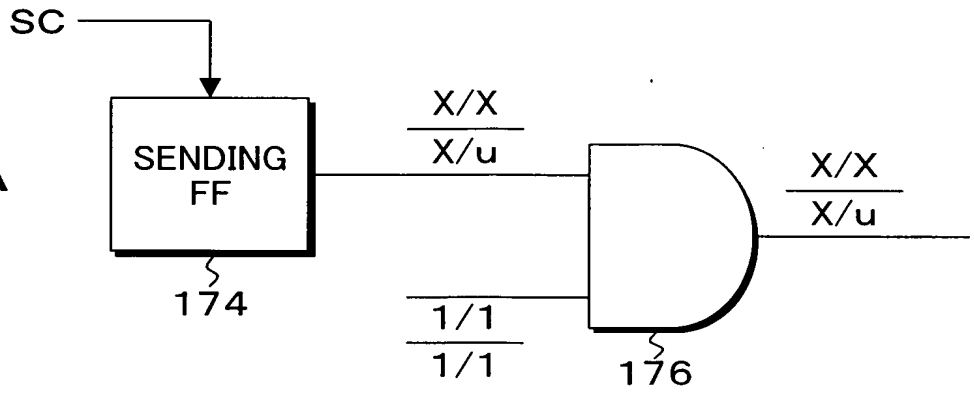


FIG. 21B

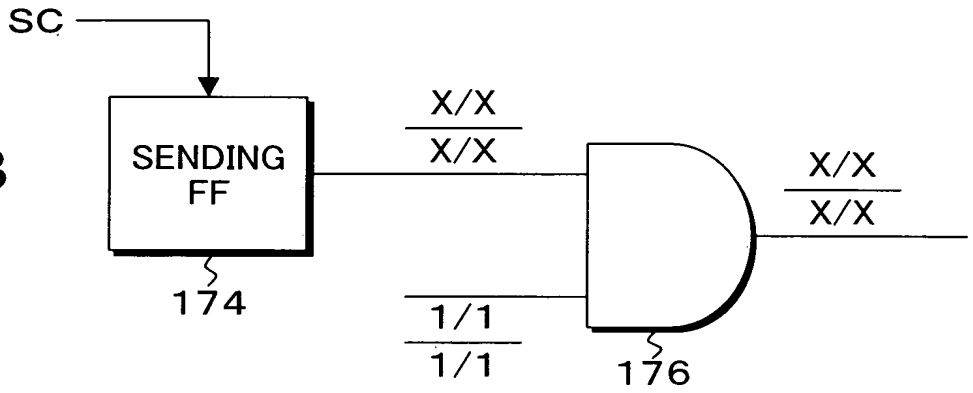
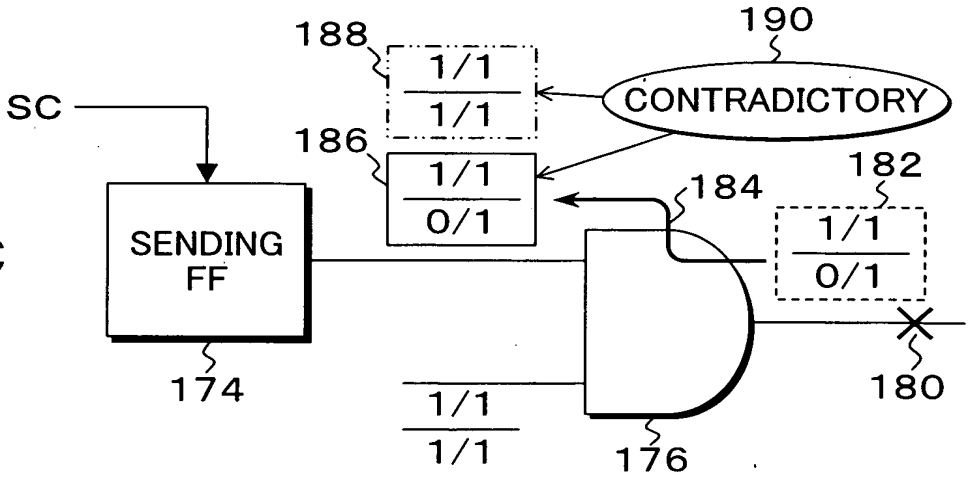


FIG. 21C



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Inventor: Daisuke MARUYAMA
Appln. No.: Unknown
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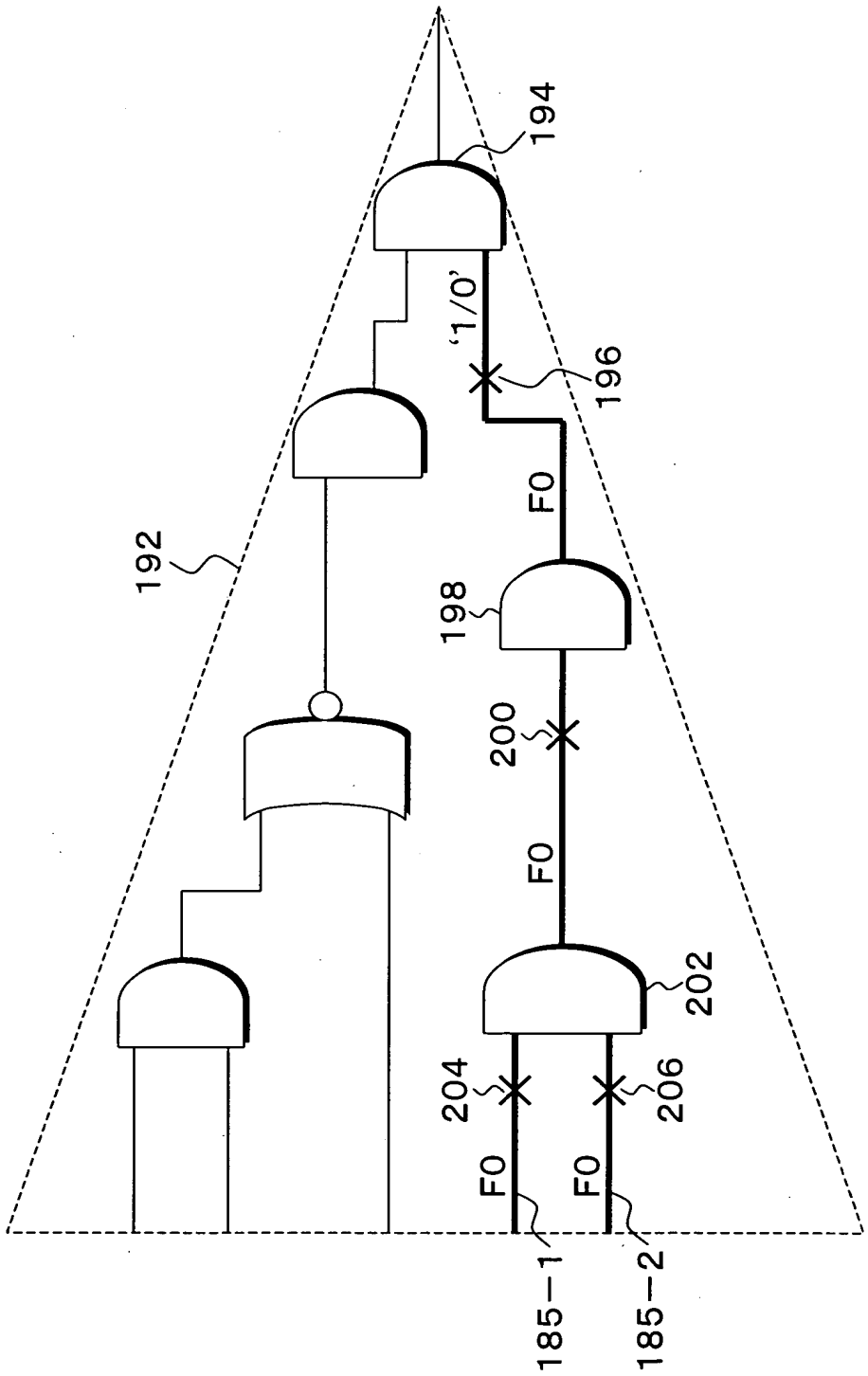
FIG. 22



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Inventor: Daisuke MARUYAMA
Appln. No.: Unknown
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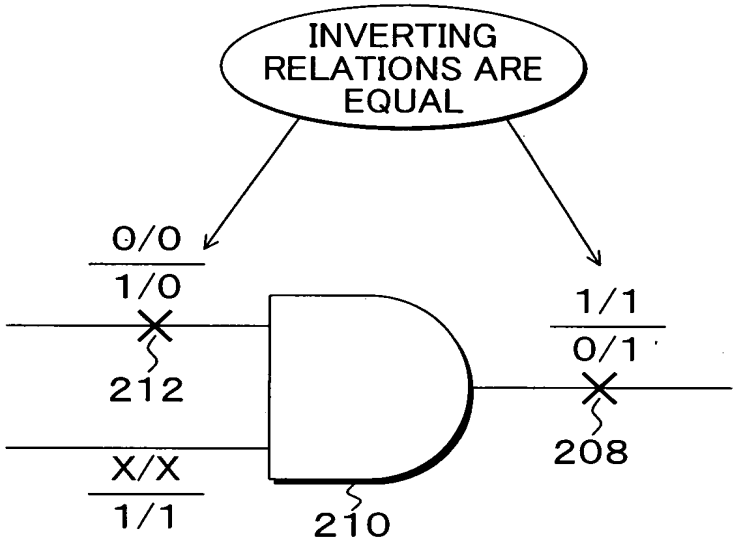
FIG. 23



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Inventor: Daisuke MARUYAMA
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FIG. 24A

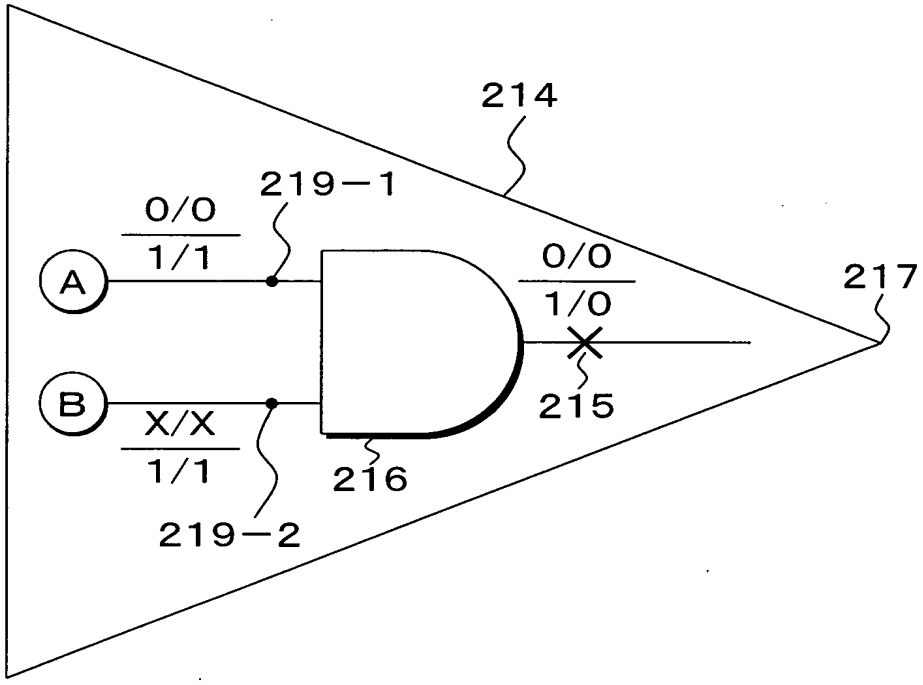
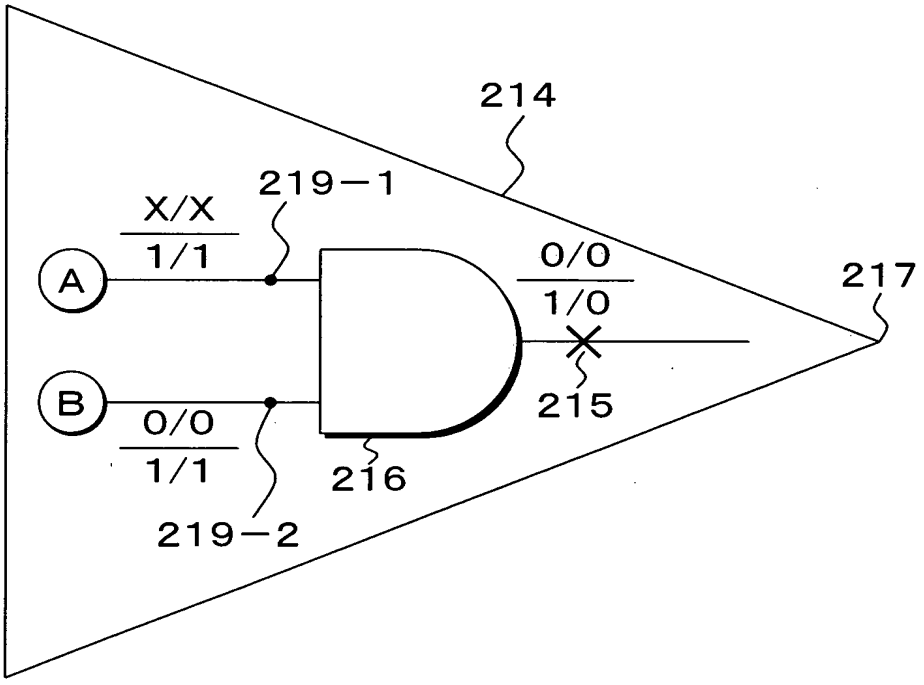


FIG. 24B



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Inventor: Daisuke MARUYAMA
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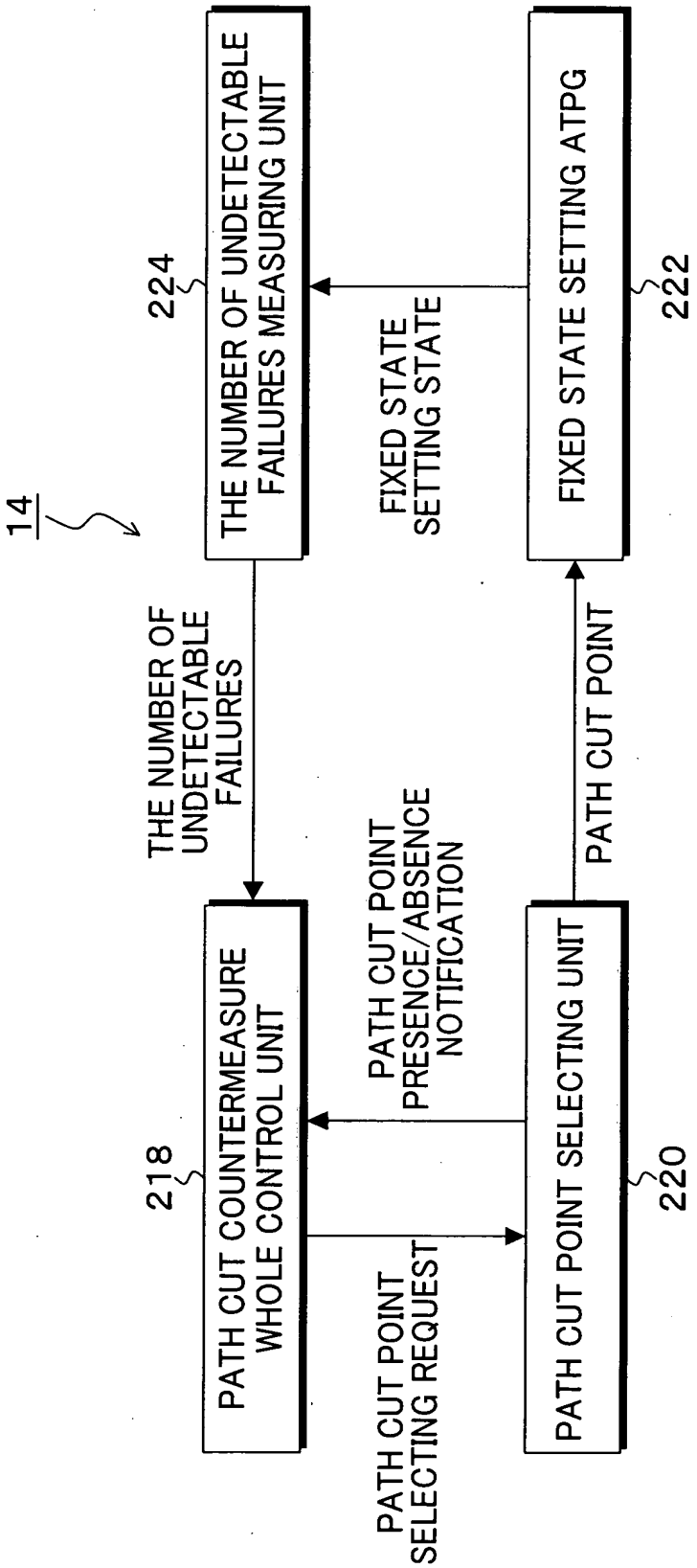
FIG. 25



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Inventor: Daisuke MARUYAMA
Appln. No.: Unknown
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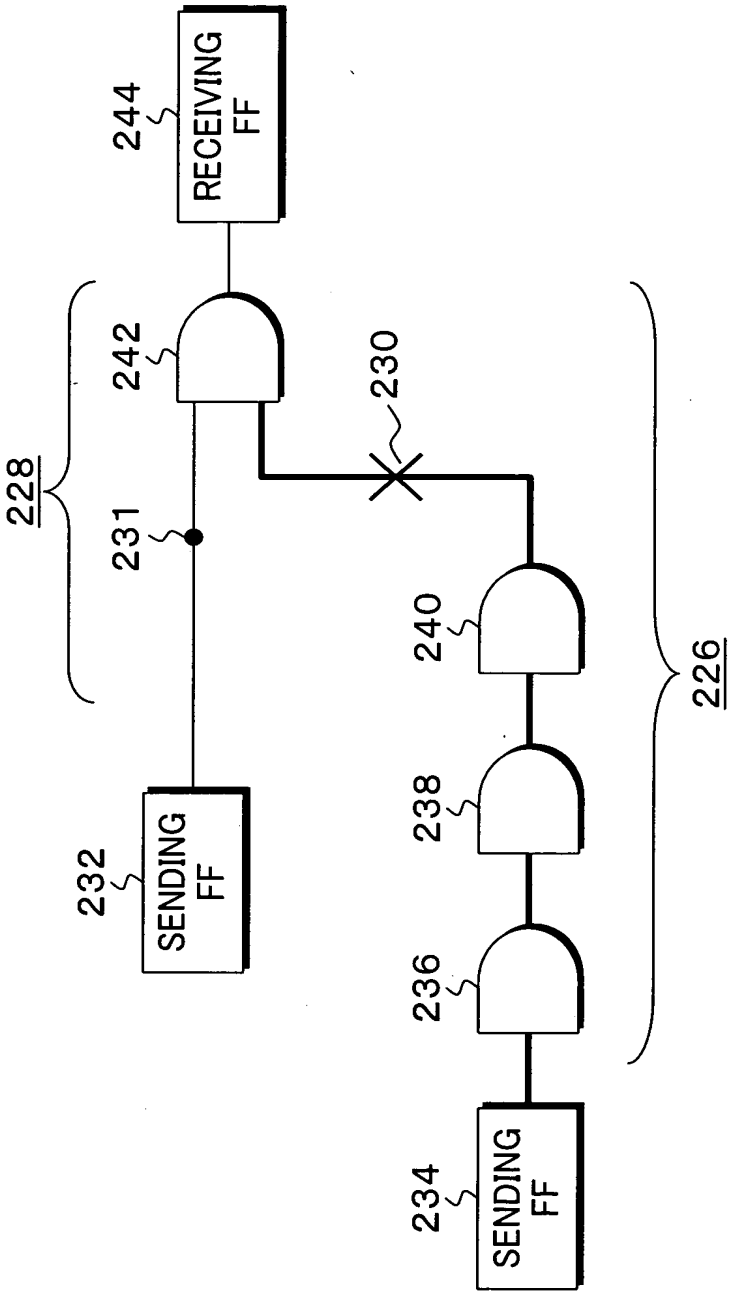
FIG. 26



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Inventor: Daisuke MARUYAMA
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FIG. 27A

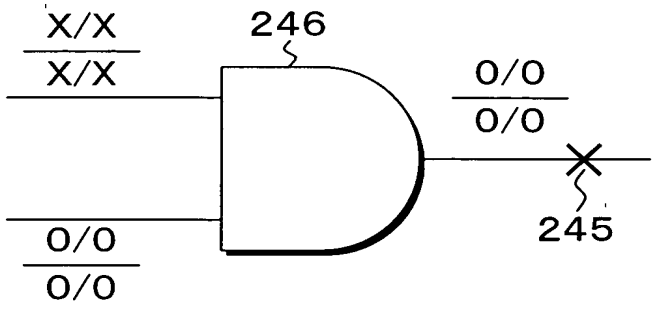
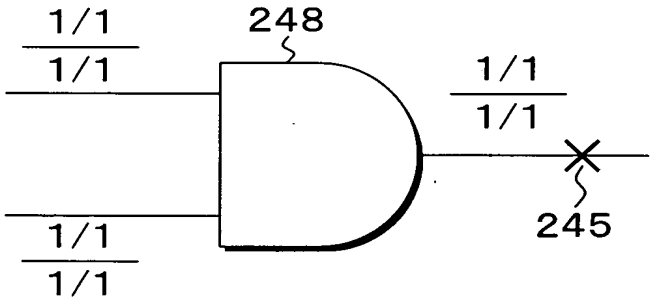


FIG. 27B



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Inventor: Daisuke MARUYAMA
Appln. No.: Unknown
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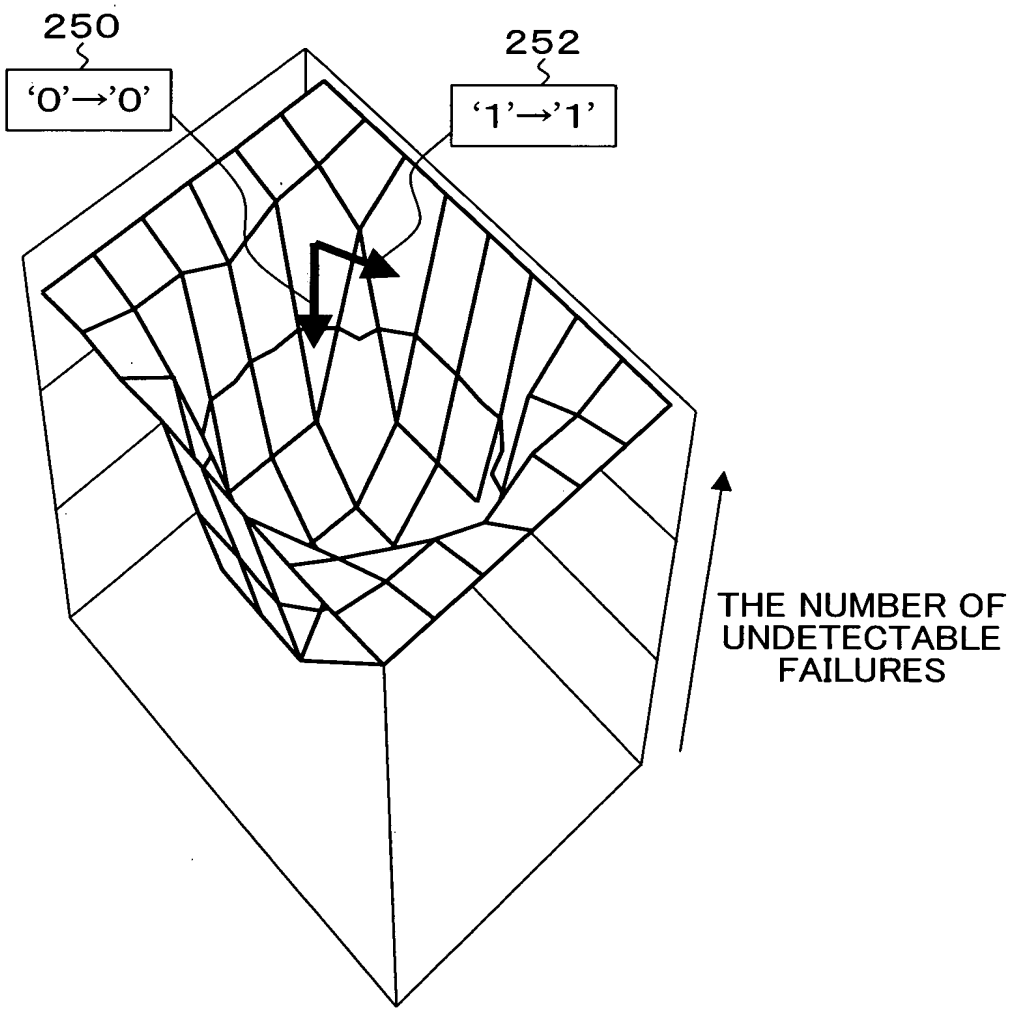
FIG. 28



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Inventor: Daisuke MARUYAMA
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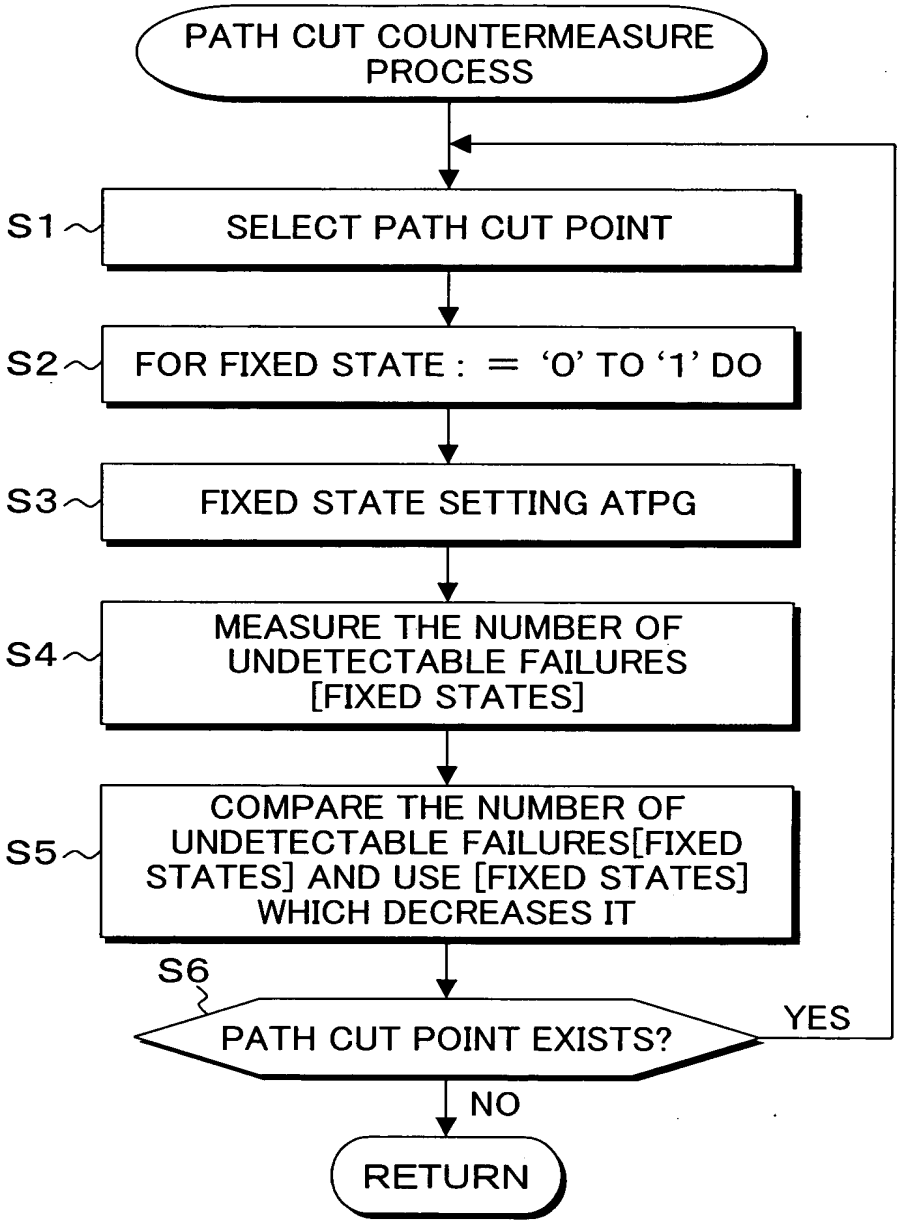
FIG. 29



Title: INTEGRATED CIRCUIT TESTING METHOD, PROGRAM, STORING MEDIUM, AND APPARATUS
Inventor: Daisuke MARUYAMA
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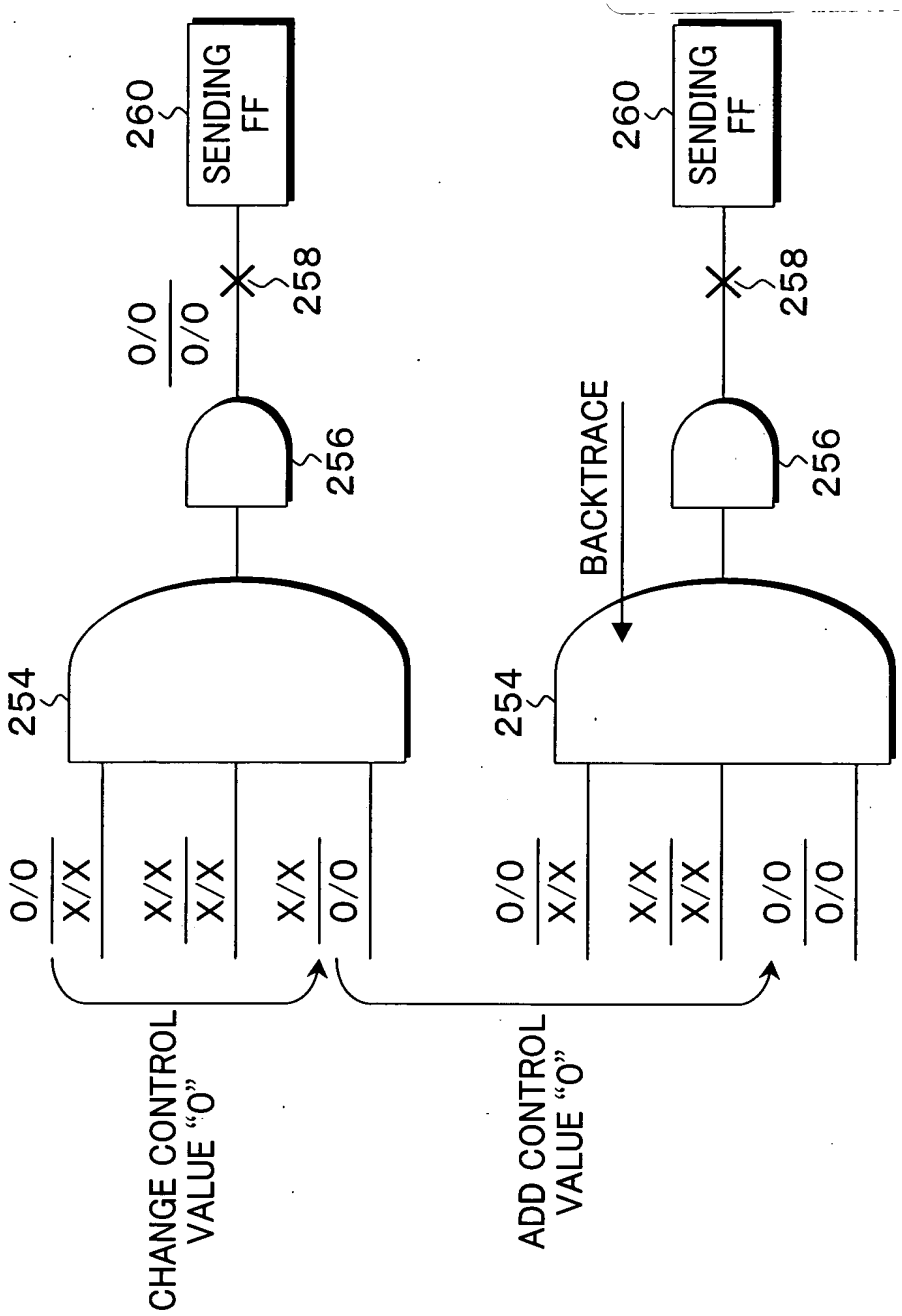

FIG. 30A

FIG. 30B

Title: INTEGRATED CIRCUIT TESTING METHOD, PROGRAM, STORING MEDIUM, AND APPARATUS
Inventor: Daisuke MARUYAMA
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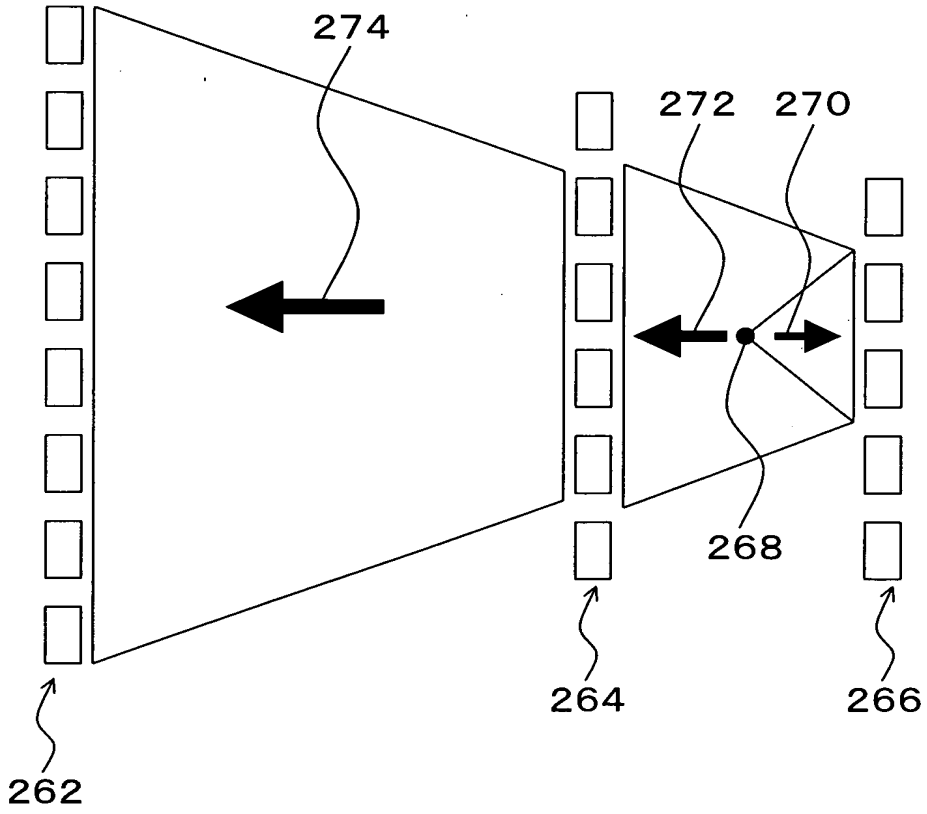
FIG. 31



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Inventor: Daisuke MARUYAMA
Appln. No.: Unknown
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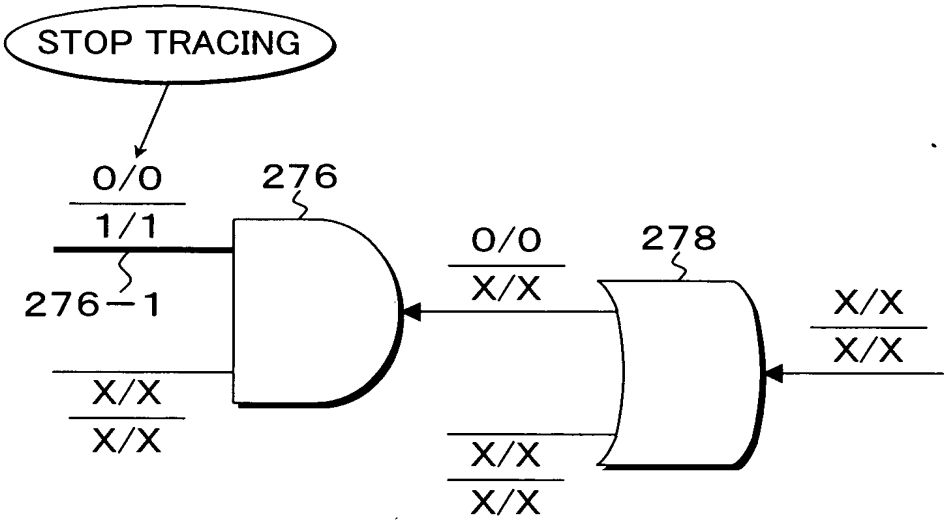
FIG. 32



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Inventor: Daisuke MARUYAMA
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FIG. 33